

S/N 09/434082

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kevin J. Ryan	Examiner:	James Peikari
Serial No.:	09/434082	Group Art Unit:	2186
Filed:	November 5, 1999	Docket:	303.306US2
Title:	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS		

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/434587 6292877	November 5, 1999	303.306US3	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
09/434654	November 5, 1999	303.306US4	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
09/434731 6418495	November 5, 1999	303.306US5	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
09/434248 6247070	November 5, 1999	303.306US6	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS

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09/225970 6172893	January 5, 1999	303.538US1	DRAM WITH INTERMEDIATE STORAGE CACHE AND SEPARATE READ AND WRITE I/O
09/756622 6466507	January 8, 2001	303.538US2	DRAM WITH INTERMEDIATE STORAGE CACHE AND SEPARATE READ AND WRITE I/O

Respectfully submitted,

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17 Feb '04

By


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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17 day of February, 2004.

Name



Signature

